WHAT IS CLAIMED IS:

1. A synchronous integrated circuit device having an output bus for outputting a plurality of output signals, comprising:

a clock input buffer configured to receive a system clock signal and to generate a buffered clock signal;

a delay line coupled to the clock input buffer, the delay line configured to receive the buffered clock signal and to generate a delayed clock signal;

an output circuit coupled to the delay line, the output circuit including a plurality of output signal paths configured to output the plurality of output signals synchronously with the system clock signal by using the delayed clock signal; and

wherein at least one of the output signal paths includes a delay circuit and an output buffer coupled to the delay circuit, each delay circuit configured to provide a programmable delay to the delayed clock signal to generate a unique delayed clock signal which is used for clocking an output signal into the respective output buffer.

2. The device of claim 1, wherein the programmable delay provided by each delay circuit is programmed to decrease output skew across the output signals.

3. The device of claim 1, wherein the clock input buffer provides a first delay, each output signal path provides a second delay, and the delay line provides a third delay based upon a delay model of the sum of the first delay and the second delay.

4. The device of claim 1, further comprising a phase detector to control the delay line based upon a phase difference between the buffered clock signal and a signal generated by applying a delay model to the delayed clock signal.

5. The device of claim 1, wherein the programmable delay provided by each delay circuit is programmed dynamically.

6. The device of claim 1, wherein the programmable delay provided by each delay circuit is programmed statically.

7. The device of claim 1, wherein the programmable delay provided by each delay circuit is programmed based upon output skew during operation of the device.

8. The device of claim 1, wherein the programmable delay provided by each delay circuit is programmed based upon an output skew between a first output signal that was output from the respective output signal path and a second output signal.

9. The device of claim 1, wherein the device has an initialization mode of operation wherein the output signals are toggled, and the programmable delay provided by each delay circuit is programmed during initialization operation.

10. A synchronous integrated circuit device having an output bus for outputting a plurality of output signals, comprising:

a clock input buffer configured to receive a system clock signal and to generate a buffered clock signal;

a delay locked loop (DLL) coupled to the clock input buffer and configured to receive the buffered clock signal and to generate a delayed clock signal;

an output circuit coupled to the DLL, the output circuit including a plurality of output signal paths configured to output the plurality of output signals synchronously with the system clock signal by using the delayed clock signal; and

wherein at least one of the output signal paths includes a delay circuit and an output buffer coupled to the delay circuit, each delay circuit configured to provide a programmable delay to the delayed clock signal to generate a unique delayed clock signal which is used for clocking an output signal into the respective output buffer.

11. The device of claim 10, wherein the programmable delay provided by each delay circuit is programmed to decrease output skew across the output signals.

12. The device of claim 10, wherein the clock input buffer provides a first delay, each output signal path provides a second delay, and the DLL provides a third delay based upon a delay model of the sum of the first delay and the second delay.

13. The device of claim 10, wherein the DLL includes a delay line coupled between the clock input buffer and the output circuit, and a phase detector to control the delay line based upon a phase difference between the buffered clock signal and a DLL clock signal generated by applying a delay model to the delayed clock signal.

14. The device of claim 13, wherein the DLL also includes a clock driver circuit coupled between the delay line and output circuit, the clock driver circuit configured to drive the delayed clock signal to each of the plurality of output signal paths.

15. The device of claim 10, wherein the DLL comprises a digital DLL.

16. The device of claim 10, wherein the DLL comprises an analog DLL.

17. A synchronous integrated circuit device having an output bus for outputting a plurality of output signals, comprising:

a clock input buffer configured to receive a system clock signal and to generate a buffered clock signal;

a delay line coupled to the clock input buffer, the delay line configured to receive the buffered clock signal and to generate a delayed clock signal;

an output circuit coupled to the delay line, the output circuit including a plurality of output signal paths configured to output the plurality of output signals synchronously with the system clock signal by using the delayed clock signal; and

wherein the output signal paths each includes a variable delay circuit and an output buffer coupled to the delay circuit, each delay circuit configured to provide an independent variable delay to the delayed clock signal to generate a unique delayed clock signal for clocking an output signal into the respective output buffer.

18. The device of claim 17, wherein the variable delay provided by each of the delay circuits is determined so as to decrease output skew across the output signals.

19. The device of claim 17, wherein the clock input buffer provides a first delay, the output signal paths provide a second delay, and the delay line provides a third delay based upon a delay model of the sum of the first delay and the second delay.

20. The device of claim 17, further comprising a clock driver circuit coupled between the delay line and the output circuit, the clock driver circuit configured to drive the delayed clock signal to each of the plurality of output signal paths.

21. The device of claim 17, wherein the independent variable delay provided by each variable delay circuit is dynamically determined.

22. The device of claim 17, wherein the independent variable delay provided by each variable delay circuit is statically determined.

23. The device of claim 17, wherein the independent variable delay provided by each variable delay circuit is based upon output skew measured during operation.

24. The device of claim 17, wherein the independent variable delay provided by each variable delay circuit is based upon output skew between a first output signal that is output from the respective output signal path and a second output signal.

25. The device of claim 17, wherein the device has an initialization mode of operation wherein the output signals are toggled, and the independent variable delay provided by each delay circuit is programmed during initialization operation.

26. The device of claim 17, wherein one of the output signal paths is the slowest output signal path, and the variable delay provided by each of the delay circuits is individually

programmed based upon the slowest output signal path so as to align the plurality of output signals, thereby decreasing skew across the output signals.

27. The device of claim 17, wherein one of the output signal paths is defined as a reference output signal path, the delay circuit for the reference output signal path provides a midpoint delay, and the delay circuits for the remaining output signal paths provide less or more than the midpoint delay if the corresponding output signal path is slower or faster than the reference output signal path, respectively.

28. A synchronous memory device having an output data bus for outputting a plurality of output data signals in response to a data read command, comprising:

a clock input buffer configured to receive a system clock signal and to generate a buffered clock signal;

a delay line coupled to the clock input buffer, the delay line configured to receive the buffered clock signal and to generate a delayed clock signal;

an output circuit coupled to the delay line, the output circuit including a plurality of output data paths configured to output the plurality of output data signals synchronously with the system clock signal by using the delayed clock signal; and

wherein the output data paths each includes a variable delay circuit and an output buffer coupled to the variable delay circuit, each delay circuit configured to provide an independent variable delay to the delayed clock signal to generate a unique delayed clock signal used for clocking data into the respective output buffer.

29. The memory device of claim 28, wherein the variable delays provided by the delay circuits are determined so as to decrease skew across the output data signals.

30. A double data rate (DDR) synchronous dynamic random access memory (SDRAM) device having an output bus for outputting a plurality of output data signals and a data strobe signal in response to a data read command, comprising:

a clock input buffer configured to receive a system clock signal and to generate a

buffered clock signal;

a delay line coupled to the clock input buffer, the delay line configured to receive the buffered clock signal and to generate a delayed clock signal;

an output circuit coupled to the delay line, the output circuit including a plurality of output signal paths configured to output the plurality of output data signals and the data strobe signal synchronously with the system clock signal by using the delayed clock signal, in response to the data read command; and

wherein at least one of the output signal paths includes a delay circuit and an output buffer coupled to the delay circuit, each delay circuit configured to provide an independent delay to the delayed clock signal to generate a unique delayed clock signal which is used for clocking an output signal into the respective output buffer.

31. The DDR SDRAM device of claim 30, wherein the delay provided by each delay circuit decreases skew across the output data signals and data strobe signal.

32. The DDR SDRAM device of claim 30, wherein the clock input buffer provides a first delay, each output signal path provides a second delay, and the delay line provides a third delay based upon a model of the first plus the second delay.

33. The DDR SDRAM device of claim 30, further comprising a phase detector to control the delay line based upon a phase difference between the buffered clock signal and a signal generated by applying a delay model to the delayed clock signal.

34. The DDR SDRAM device of claim 30, further comprising a clock driver circuit coupled between the delay line and the output circuit, the clock driver circuit configured to drive the delayed clock signal to each of the output signal paths.

35. The DDR SDRAM device of claim 34, wherein the clock driver circuit generates rising-edge and falling-edge delayed clock signals, and the output circuit outputs first and second data words synchronously with rising and falling edges of the system clock signal

using the rising-edge and falling-edge delayed clock signals.

36. The DDR SDRAM device of claim 30, wherein the independent delay provided by each delay circuit is dynamically determined.

37. The DDR SDRAM device of claim 30, wherein the independent delay provided by each delay circuit is determined based upon a measured output skew.

38. The DDR SDRAM device of claim 30, wherein the device has an initialization mode of operation wherein the output data signals and the data strobe signal are toggled, and the independent delay provided by each delay circuit is programmed based upon output skew during operation in the initialization mode.

39. The DDR SDRAM device of claim 30, wherein one of the output signal paths is the slowest output signal path, and the independent delay provided by each delay circuit is individually programmed based upon the slowest output signal path.

40. The DDR SDRAM device of claim 30, wherein one output signal path acts as a reference output signal path, the delay circuit for the reference output signal path provides a midpoint delay, and the delay circuits of the other output signal paths provide less or more than the midpoint delay if the corresponding output signal path is slower or faster than the reference output signal path, respectively.

41. The DDR SDRAM device of claim 40, wherein the reference output signal path is the output signal path that is configured to output the data strobe signal.

42. A DDR SDRAM device having an output bus for outputting a plurality of data signals and a data strobe signal in response to a read command, comprising:

a clock input buffer configured to receive a system clock signal and to generate a buffered clock signal;

a DLL coupled to the clock input buffer and configured to receive the buffered clock signal and to generate at least one delayed clock signal;

an output circuit coupled to the DLL, the output circuit including a plurality of output signal paths configured to output the plurality of data signals and the data strobe signal synchronously with the system clock signal using the at least one delayed clock signal, in response to the read command; and

wherein at least one of the output signal paths includes a delay circuit and an output buffer coupled to the delay circuit, each delay circuit configured to provide an independent delay to the delayed clock signal to generate a unique delayed clock signal which is used for clocking an output signal into the respective output buffer.

43. A method of outputting a plurality of output signals on an output bus of a synchronous integrated circuit device with decreased output skew, comprising:

receiving a system clock signal;

delaying the system clock signal to generate a delayed clock signal;

applying the delayed clock signal to a plurality of output signal paths;

in each of the output signal paths, using the delayed clock signal to output the plurality of output signals synchronously with the system clock signal; and

in at least one of the output signal paths, providing a programmable delay to the delayed clock signal to generate a unique delayed clock signal which is used for clocking an output signal out from the respective output signal path.

44. The method of claim 43, wherein each programmable delay is provided to decrease output skew across the output signals.

45. The method of claim 43, wherein receiving the system clock signal includes buffering the system clock signal.

46. The method of claim 43, wherein delaying the system clock signal includes detecting a phase difference between the system clock signal and a signal generated by

applying a delay model to the delayed clock signal, and using the detected phase difference to control the amount of delay provided to the system clock signal.

47. The method of claim 43, wherein delaying the system clock signal includes applying the system clock signal as an input signal to a DLL.

48. The method of claim 43, wherein providing each programmable delay takes place dynamically.

49. The method of claim 43, wherein providing each programmable delay includes determining output skew during an initialization mode of device operation.

50. The method of claim 43, wherein applying the delayed clock signal to the plurality of output signal paths includes driving the delayed clock signal, thereby increasing fanout of the delayed clock signal.

51. A method of outputting a plurality of output signals on an output bus of a synchronous integrated circuit device with decreased output skew, comprising:

receiving a system clock signal;

delaying the system clock signal to generate a delayed clock signal;

applying the delayed clock signal to a plurality of output signal paths;

in each of the output signal paths, using the delayed clock signal to output the plurality of output signals synchronously with the system clock signal; and

in each of the plurality of output signal paths, providing an independent variable delay to the delayed clock signal to generate a unique delayed clock signal for use in clocking an output signal out from the respective output signal path.

52. The method of claim 51, wherein each independent variable delay is provided to decrease output skew across the output signals.

53. The method of claim 51, further comprising determining the output signal path which is the slowest output signal path, wherein providing each variable delay is based upon the slowest output signal path so as to align the output signals.

54. The method of claim 51, further comprising defining one of the output signal paths as a reference output signal path, wherein providing the variable delay for the reference output signal path includes providing a midpoint delay, and providing the variable delay for the remaining output signal paths includes providing less or more than the midpoint delay if the corresponding output signal path is slower or faster than the reference output signal path, respectively.

55. A method of outputting a plurality of output data signals on an output data bus of a synchronous memory device in response to a read command, comprising:

receiving a system clock signal;

delaying the system clock signal to generate a delayed clock signal;

applying the delayed clock signal to a plurality of output data paths;

in each of the output data paths, using the delayed clock signal to output the plurality of output data signals synchronously with the system clock signal; and

in each of the output data paths, providing a programmable delay to the delayed clock signal to generate a unique delayed clock signal which is used for clocking an output data signal out from the respective output data path.

56. The method of claim 55, wherein each programmable delay is provided to decrease output data skew across the output data signals.

57. A method of outputting a plurality of output data signals and a data strobe signal on an output bus of a DDR SDRAM device in response to a read command, comprising:

receiving a system clock signal;

delaying the system clock signal to generate a delayed clock signal;

applying the delayed clock signal to a plurality of output signal paths;

in the plurality of output signal paths, using the delayed clock signal to output the plurality of output data signals and the data strobe signal synchronously with the system clock signal in response to the read command; and

in at least one of the output signal paths, providing a variable delay to the delayed clock signal to generate a unique delayed clock signal which is used for clocking an output signal out from the respective output signal path.

58. The method of claim 57, wherein each variable delay is provided to decrease output skew across the output data signals and the data strobe signal.

59. The method of claim 57, wherein receiving the system clock signal includes buffering the system clock signal.

60. The method of claim 57, wherein delaying the system clock signal includes detecting a phase difference between the system clock signal and a signal generated by applying a delay model to the delayed clock signal, and using the detected phase difference to control the amount of delay provided to the system clock signal.

61. The method of claim 57, wherein delaying the system clock signal includes applying the system clock signal as an input signal to a DLL.

62. The method of claim 57, wherein providing each variable delay takes place dynamically.

63. The method of claim 57, wherein providing each variable delay includes determining output skew during an initialization mode of device operation.

64. The method of claim 57, wherein applying the delayed clock signal to the plurality of output signal paths includes driving the delayed clock signal, thereby increasing fanout of the delayed clock signal.

65. The method of claim 57, wherein applying the delayed clock signal to the plurality of output signal paths includes generating rising-edge and falling-edge delayed clock signals used for outputting first and second data words synchronously with rising and falling edges of the system clock signal.

66. The method of claim 57, further comprising determining the output signal path which is the slowest output signal path, wherein providing each variable delay is based upon the slowest output signal path.

67. The method of claim 57, further comprising defining one of the output signal paths as a reference output signal path, wherein providing the variable delay for the reference output signal path includes providing a midpoint delay, and providing the variable delay for the remaining output signal paths includes providing less or more than the midpoint delay if the corresponding output signal path is slower or faster than the reference output signal path, respectively.

68. An apparatus for outputting an output signal on an output bus of a synchronous integrated circuit device with decreased output skew, comprising:

an input circuit for receiving a system clock signal;

a delay line coupled to the input circuit for delaying the system clock signal; and

an output circuit coupled to the delay line for outputting an output signal, the output circuit including a programmable delay circuit for providing a programmable delay to the delayed system clock signal for use in clocking out the output signal.

69. An apparatus for outputting a plurality of output signals on an output bus of a synchronous integrated circuit device with decreased output skew, comprising:

an input circuit for receiving a system clock signal;

a delay line coupled to the input circuit for delaying the system clock signal; and

an output circuit coupled to the delay line for outputting a plurality of output signals, the output circuit including at least one programmable delay circuit for providing a

programmable delay to the delayed system clock signal for use in clocking out at least one of the output signals with decreased skew across the bus.

70. An apparatus for outputting a DDR output signal on an output node of a synchronous DDR integrated circuit device, comprising:

an input circuit for receiving a system clock signal;

a delay line coupled to the input circuit for delaying the system clock signal; and

an output circuit coupled to the delay line for outputting the output signal, the output circuit including first and second delay circuits to provide first and second programmable delays to rising and falling edges of the delayed system clock signal, respectively, for clocking out first and second signals on the output node.